Exhibit A to Response to Office Action:

Class Notes from vco.ett.utu.fi/courses/ETT_2015/kalvot/luento4.pdf

CS152
Computer Architecture and Engineering

Lecture 5: Cost and Design

September 10, 1997

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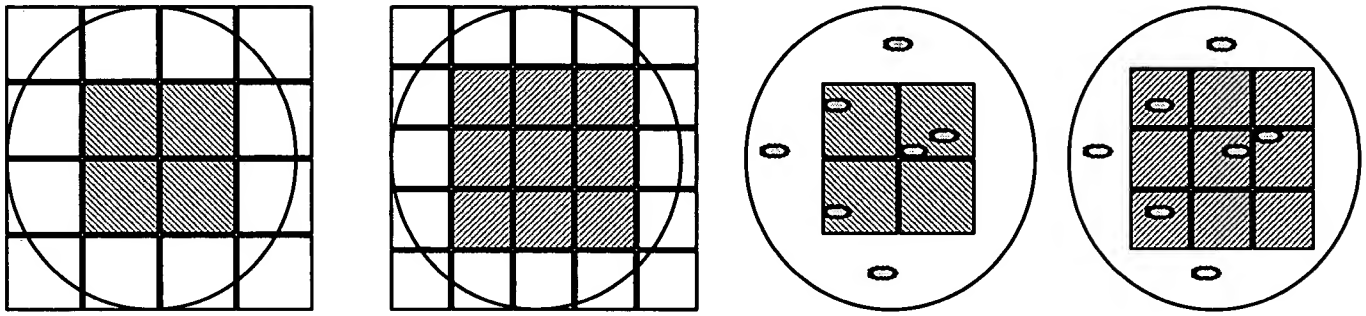
lecture slides: http://www-inst.eecs.berkeley.edu/~cs152/

Integrated Circuit Costs

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per Wafer} * \text{Die yield}}$$

$$\text{Dies per wafer} \sim \text{eff} \frac{\text{Wafer Area}}{\text{Die Area}}$$



$$\text{Die Yield} = \frac{\text{Wafer yield}}{\left\{ 1 + \frac{\text{Defects\_per\_unit\_area} * \text{Die\_Area}}{?} \right\}^{?}}$$

Die Cost is goes roughly with the cube of the area.